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Performance of a New MCM-D Technology Front-End Digital Readout

P. Cluzel, R. Della-Negra, M. Goyot, M. Miguet, A. Savoy-Navarro

Abstract— A EEC ESPRIT Project developed a new MCM-D packaging technology with a view to industrial, biomedical and HEP applications. The objective was to establish a cost-efficient base, made of silicon-based MCMs, that are commercially manufactured, with active substrate and ball-grid array interconnects. Among its main features are the integration of active and passive components in the substrate and the use of flip-chip technique and wafer rerouting, leading to a size reduction of the interconnects and also a reduction of power consumption and of noise. The demonstrator built to show the potentiality of this technique is a prototype of a fast digital readout front-end electronics. It combines a low-noise and fast preamplifier and a fast and large dynamic range 12-bit ADC, thus mixing analogue and digital components. It also includes a PLL and boundary scan test cells, which are integrated in the substrate, as well as passive components. Detailed tests have been performed, showing that this demonstrator achieves very high performances in terms of noise, signal processing and imaging properties.

Keywords— MCM-D, digital readout, new I&P technology.

I. INTRODUCTION

THE EEC ESPRIT Project, called SUMMIT (Silicon sUBstrate Multi-chip Modules for Innovative products),¹ developed a new MCM-D technology. The objective of the overall project was to establish a cost-efficient, commercial manufacturing base in silicon-based MCMs with active substrates and ball grid array interconnects. The main features and advantages of this MCM-D technology are briefly described in Section 2. A demonstrator was built to test most of the properties and potentiality of this Interconnects and Packaging (I&P) technology. Indeed this MCM-based circuit contains the basic components of a fast front-end digital readout electronics for HEP detectors. Building such a digital readout system was one of the key-issue of this past decade in HEP experiments. It led to an active R&D and in fact, the novelty of this demonstrator is that it is the first time that such a performing readout system is designed and built using a new packaging technology, namely the MCM-D active substrate as developed by SUMMIT. The goal in using this new I&P

technology is to help confronting most of the challenges that these electronic systems are or will be encountering in present or future HEP experiments. Section 3 reviews the design and the layout of this circuit as well as its main components. The performances achieved by this MCM-based readout prototype are summarized in Section 4. In that section, the results in terms of noise, signal processing and imaging properties demonstrate the great potentiality of this new packaging technology for performing electronic systems. The prospects for using this MCM-D technology not only for HEP applications but also for industrial and biomedical applications are briefly discussed in the conclusion.

II. THE MCM-D SUMMIT TECHNOLOGY

This section briefly recalls the main features of the developed MCM technology. It is a type-D MCM, i.e. using thin film deposition, and has an active silicon substrate. Therefore it offers as benefits no need of chips with a single active function, less discrete components for biasing, loading, decoupling and filtering; moreover, the integrated test structures improve its testability. All this reduces its cost. Figure 1 shows a schematic transverse view of the SUMMIT MCM-D technology.

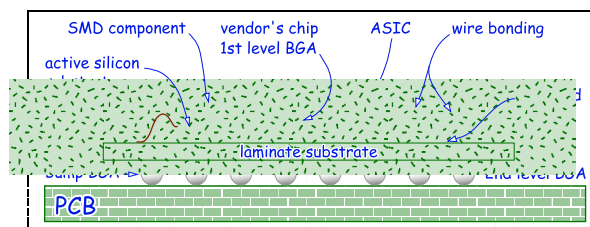


Fig. 1. Schematic transverse view of the SUMMIT MCM-D technology

This technique allows chips/ASICs to be mounted whether they are encapsulated or provided in wafer form. If encapsulated, they will be, as usual, wired-bonded on the substrate. If they are delivered as wafers, they will be connected using the flip-chip technique with wafer-rerouting and the BGA interconnects. The use of the flip-chip technique and wafer rerouting is beneficial as it gives a size reduction due to the shortening in length of the interconnects and also a decrease of the power consumption. The wafer rerouting is also beneficial as it reduces the connection between the silicon substrate and the PCB base, to a single wire-bonding step. There is no need to modify the die layout.

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Figure 2 details the various layers of the MCM cross-view and their respective widths, up to and including the second level of BGAs that connect the MCM to the PCB base. Higher density, higher functionality and testability,

Fig. 2. Schematic transverse view of the active substrate of the SUMMIT MCM-D, showing the detailed structure of the various layers. The Si layer is the CMOS back-end.

III. THE MCM-BASED DEMONSTRATOR: LAYOUT AND COMPONENTS

The schematic block-diagram of this device (Fig. 3) shows the two main components, namely a low-noise and fast preamplifier followed by an analog-to-digital converter. In order to meet the challenges of the present and future experiments, the circuit must be high speed (i.e. of the order of 10 to 40 MHz) and low-noise, with a highly performing analog component, a high-speed and large dynamic range digital component; it must also be a high-rate and well-synchronized system, with high density and good testability for full reliability and low cost.

The analog part consists of the LNCP52-VFE amplifier, made in UHF-Harris bipolar technology by ALCATEL; this ASIC has been fully tested and it is described

Fig. 3. Schematic block diagram of the MCM-based demonstrator, prototype of a fast front end digital readout

The detailed layout of this device is shown in Fig. 4. The size of the silicon substrate is $15.3 \times 16.8 \text{ mm}^2$ and that of the PCB base is $30 \times 30 \text{ mm}^2$. The main challenges to be

Fig. 4. Layout of the demonstrator

met by this MCM are first that it includes highly performing devices, and its environment must therefore preserve in particular the low noise, the high speed, the large dynamic range, the easy testability to ensure the reliability, and the low power consumption or easy cooling. Secondly it mixes analog and digital circuits, with two different bipolar technologies, and different voltages must therefore be applied to each of them. Finally one should keep in mind that this device, being a demonstrator, was designed to make it possible to test its main components, i.e. the analog and the digital parts, either separately or together. To do so, one needs to make a compromise between asking for a high testability or degrading, in some respects, the intrinsic performances of this prototype (see next section). Figure 5 is

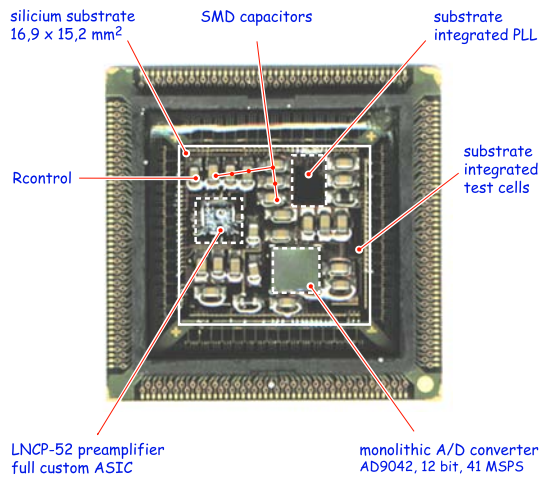


Fig. 5. Photograph of the uncovered MCM-based demonstrator, with the description of the different components and the way they are integrated or connected to the active substrate.

a photograph of the uncovered MCM-based demonstrator: it shows the various components that are integrated in the substrate, the various techniques of bonding that are used to connect each ASIC or die to the substrate, the details of the floor plane, the passive components that are surface-mounted and the ones that are integrated in the substrate.

IV. PERFORMANCES OF THE MCM-BASED DEMONSTRATOR

The purpose was to test either separately the analog and the digital parts or both together, i.e. the whole readout chain. The prototype itself, the evaluation board and the overall test bench were each designed to make this possible.

A. Description of the test-bench

The layout of the MCM-based demonstrator allows a direct access to the output of the LNCP52 preamplifier as well as the input of the ADC. This is done at the cost of having an external wired connection between the preamplifier output and the input of the ADC, instead of a direct

connection inside the substrate between the two I/O's. Of course this deteriorates a little the performance of the overall readout chain.

The evaluation board was aimed at providing the necessary environment for the functionality tests of this MCM technology as well as for the performance tests. It is a $110 \times 110 \text{ mm}^2$ and four-layer PC board with a Ni-Au electroplated finish. Figure 6 shows a photograph of this test card. In order to allow the test of several prototyped

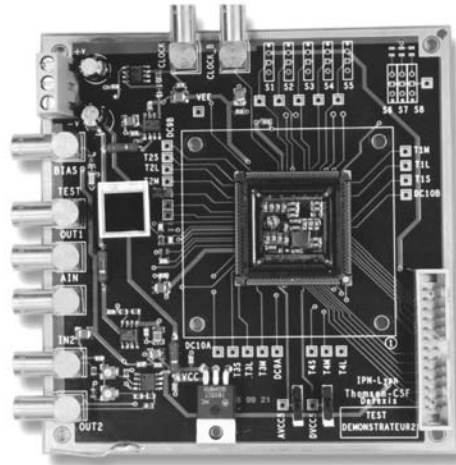


Fig. 6. Photograph of the evaluation board.

MCM circuits on the same evaluation board, each prototype is mounted on a fully custom socket of the compression type. It consists of an elastomer layer with a contact resistor of $\leq 0.1 \Omega$, placed in between the external BGAs of the MCM device and the PC board. It ensures a good and uniform contact. The top part of the socket is a plastic cover with a moulded MCM shape. The price paid for the test flexibility provided by the socket is a 27 mm increase in length of the connection between the MCM outputs and the elements on the test board. This again slightly degrades the response of the overall chain.

The board is auto-supplied in voltages. In fact it is supplied with +12 V, 0 and -12 V and it makes from these voltages all the voltages that are needed to allow the functioning of the different devices included on the MCM, i.e. +5 V, -5.2 V, +8 V and -3 V. It also includes test elements and test inputs, in particular a S3590 Hamamatsu photodiode that acts as a photodetector to test the functioning of the readout circuit in real-life conditions. It may be replaced by a silicium detector. Besides, several test inputs are available externally. There is a possibility to inject a charge, i.e. an analog pulse mimicking a real detector pulse. Other types of test inputs are available to characterize the technology using daisy-chains on each of the four sides of the board.

Moreover, there are three additional devices on the evaluation board. One is a fast preamplifier, CLC425 (Com-

linear) of National Semiconductor, which can work with a positive or negative gain (direct or inverted). Another test device consists in a test capacitance charge injection of 12 pF (12 pC/V), which allows a large dynamic range to be covered. An external RC component allows us to adjust the integration length of the signal, and therefore its peaking time. Finally, two clock inputs permit to send the clock signals needed for the functioning of the PLL and of the ADC.

The overall test bench sketched in Fig. 7 is VXI/VME and LabVIEW-based. It consists of a PC running software

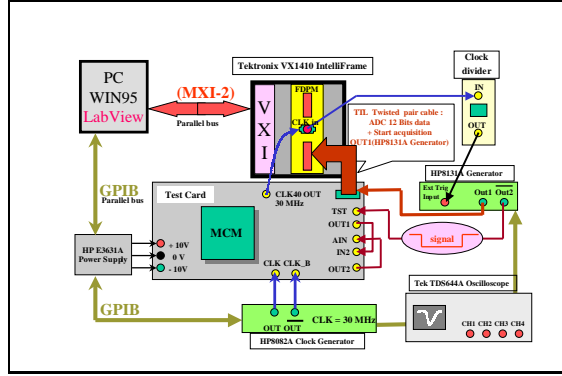


Fig. 7. schematic view of the LabVIEW-based test bench

developed using Windows95 and LabVIEW package from National Instruments, an interface to VME, a GPIB branch for controlling instruments (namely the HPE3631A power supply and the HP8082A clock generator), a VXI crate housing a Fast Dual Port Memory (FDPM). The FDPM is used as a data buffer and allows up to 32-bit words and a depth of 128 Kwords. The output of the AD9042 on the evaluation board is connected to the FDPM where are stored the data that are then processed in the LabVIEW-PC, via a TTL twisted-pair cable.

The clock signals used to synchronize the functioning of the AD9042 and the PLL are handled via GPIB connections by the LabVIEW-PC with a clock frequency of 30 MHz corresponding to the maximum running frequency of the PLL.

B. Tests of the Analog Part

The analog part consists of a fast, low-noise preamplifier using Harris Semiconductor UHF1 bipolar transistor process for detector capacitances in the range of 10 to 100 pF. It is subdivided into three separate functions: low-noise preamplifier, buffer and DC differential amplifier. The power dissipation for the whole circuit at nominal bias voltage is 13 mW. Figure 8 shows a schematic block diagram of this device and of the available tests I/O's. This preamplifier has been extensively tested using in particular an optimized test environment [3]. A series of tests were repeated with the device mounted on the MCM and compared with those where the preamplifier is not mounted on an MCM.

B.1 Electrical Characteristics

A certain number of the voltage nodes are made available on the evaluation board. Thus, when the LNCP52 is powered on, all the voltage nodes are tested. The values obtained are compared with those obtained when the LNCP52 is not mounted on an MCM. A pretty good agreement is obtained, showing that the chip is electrically ready to work in its MCM environment, as it was in an optimized test environment.

B.2 Tests of the Signal Characteristics

The response signal from the LNCP52 is tested in various conditions. First, with the internal DC feedback on, plus the internal feedback component of the integrated ASIC, a charge is injected at the test entrance of the circuit (see Fig. 8).

Four different input levels, i.e. charges, are sent, cor-

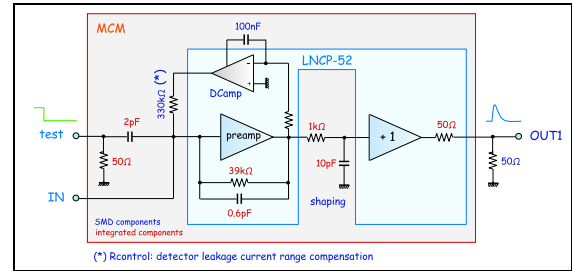


Fig. 8. Block diagram of the test system for the analog part only

responding respectively to 3.12, 0.3, 0.03 and 0.01 pC. An additional 12 pF capacitance at the entrance "IN" mimicks the effect of the detector capacitance, when a detector is connected to the circuit (real-life conditions). The response signals, at the output "OUT1", obtained with the 4 different injected charges, are shown in Fig. 9. The response of

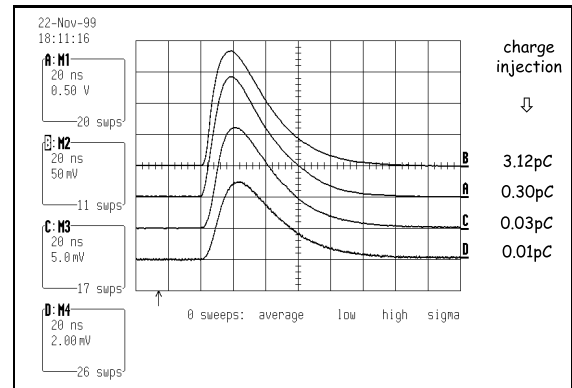


Fig. 9. Test of the analog part only

the signal varies proportionally to the amount of injected charge, thus testing the dynamic of the response signal and showing its linear behaviour, as expected. The total length of each of the four signals is quite similar, of the order of

120 nsec, and the peaking time moves slightly, by 4 to 5 nsec, when going from the signal of highest amplitude to the one of lowest. The peaking time is of the order of 20 nsec.

Moreover, the comparison of these results with those obtained when the LNCP52 is not mounted on an MCM base, shows a very good agreement between the two series of measurements [3].

B.3 Noise Studies

These tests are performed using an LT344L LeCroy digital scope. As previously, a pulse is injected with an external capacitance. The LT344L analyses on-line the output pulse after the shaping CLC425 amplification. The result is shown in Fig. 10. Corresponding to a charge injection of

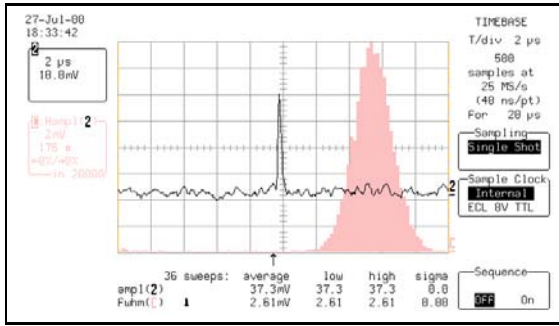


Fig. 10. Output pulse delivered by the LNCP52 device, after the shaping CLC425 amplification.

17 fC and after a shaping amplifier with a gain of 10 and a peaking time of 75 nsec, a rms noise of 3140 e⁻ is measured. Here again the obtained result is in good agreement with the one obtained when the LNCP52 is not mounted on an MCM.

When powering on the ADC, the same measurement is repeated under the same conditions: no modification due to the ADC is observed.

At this stage, we can conclude that no alteration in the performances of the analog part has been observed that would be due to the new MCM-packaging, and indeed the low-noise preamplifier works pretty well, i.e. its performances are preserved by this new packaging, even though the overall system is located in the MCM (namely: clocks, mixture of digital and analog devices, high density, external connections that have been added for test flexibility and that will not be present in the final set-up).

C. Tests of the Readout Chain

These tests are performed on the LabVIEW-based test bench (see Fig. 7). First, the functioning of the digital part is verified, independently of the analog part of the system, and then the whole readout chain response is tested. All the measurements are done with a sampling frequency of 28 MHz, for the AD9042. This ADC can work up to 40

MHz, but we chose this value of 28 MHz to stay within safe conditions for the PLL, as the PLL is limited by its present design to 30 MHz. The measurement frequency, i.e. the triggering frequency, as sent by the Out1 of the HP8131A oscilloscope, is provided by the clock divider and is equal to 1.12 kHz.

C.1 Test of the Digital Part Only

The first test consists in sending no signal at the direct entrance of the ADC and therefore in measuring the output, i.e. the intrinsic noise of this device. This “intrinsic” noise also includes, of course, some extra noise due to the test environment, i.e. in particular, the cabled connections, the clocking system and the overall digital test environment. To evaluate the rms noise, 500 samplings are taken for each trigger and the corresponding rms is then computed. This is repeated 4000 times and the corresponding histogram of the rms distribution is calculated, from which the average rms is derived with a value of 1.8 mV. This is shown in Fig. 11. A step-signal of 400 mV is

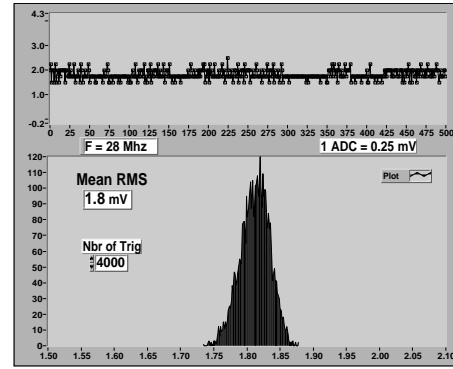


Fig. 11. Measurement of the rms noise for the ADC only

then directly sent to the input of the ADC with the sampling and the ADC frequencies mentioned above. Of the order of 10 measurements are taken for each trigger and the pedestal is subtracted from the signal. The measurements are repeated 8000 times and the FWHM of the resulting histogram gives 0.6 mV, as shown in Fig. 12.

C.2 Tests of the Overall Readout Chain

The tests of the overall readout chain are performed by sending a step pulse in the test input of the LNCP52 preamplifier; the signal is then transmitted to the ADC via an external cable. This cable directly connects the output (OUT1) of the LNCP52 device to the input (AIN) of the AD9042, through an additional amplifier stage (IN2/OUT2), namely the CLC425 amplifier that is available on the test board. This was shown in detail in Figs. 6 and 7.

The overall noise rms is measured much as for the ADC alone. The result as shown in Fig. 13, gives a mean rms

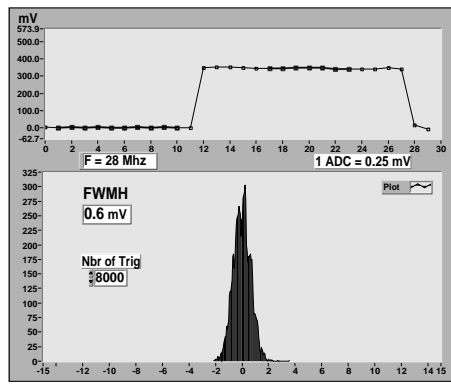


Fig. 12. Response signal of the ADC only to a step signal

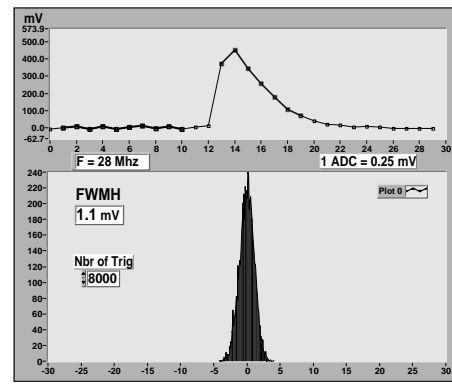


Fig. 14. Estimate of FWHM of the response of the overall chain, to a step signal of 750 mV on 50 Ω, without additional amplification stage.

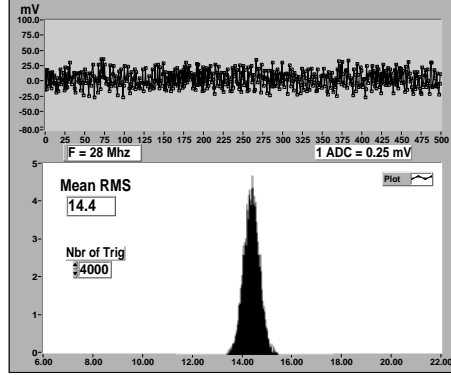


Fig. 13. Estimate of mean rms noise corresponding to the whole readout chain plus all the extra noise due to the external connections, the clocking system, and the additional external amplifier stage.

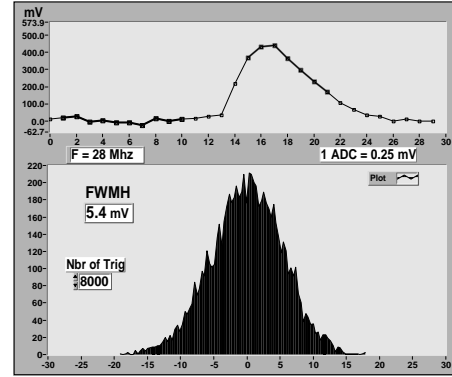


Fig. 15. Estimate of FWHM of the response of the overall chain, to a step signal of 750 mV on 50 Ω, with an additional amplification stage.

of 14.4 mV. Here one must take into account that this noise includes not only the intrinsic noise of the overall readout chain, i.e. the LNCP52 plus the AD9042 and all the internal components of the system contained in the MCM, but also the extra noise due to the external cabling, the clocking system, the CLC425 additional amplifier stage and the overall digital component of the test system.

A step pulse of 750 mV on 50 Ω is sent in the test input of the LNCP52. It is transmitted to the digitization stage without passing through an additional external amplification stage. For each trigger, 7 samplings around the peak of the impulsions are taken and subtracted from the mean of the 10 samplings taken on the baseline (i.e. the pedestal). This measurement is repeated 8000 times and the FWHM value of the obtained distribution is 1.1 mV, as derived from the LabVIEW plot in Fig. 14. The same measurement is repeated, but adding the CLC425 amplifier in the chain. The input signal is a step signal of 54 mV on 50 Ω. The result shown in Fig. 15, gives a corresponding FWHM for the response signal of 5.4 mV.

The test in linearity of the response of the whole readout chain is performed by scanning the overall available dynamic range, i.e. from 0 to 500 mV. This is done with and without the additional external amplification stage (i.e. the CLC425 amplifier). The results are reported in Fig. 16 and show a good linearity in essentially all the available dynamic range.

The fitted slopes are equal to 3.9 when the CLC425 amplifier is included, and to 0.3 when it is not.

An important property of this digital readout system is its *imaging capability*. This is tested by comparing the pulse as sampled by a digital oscilloscope (namely the TDS644A from Tektronix of 18 × 28 MHz frequency.) with the one sampled by the MCM-based digital readout with a frequency of 28 MHz. The results are reported in Fig. 17. Indeed, by exploiting the digital potentiality already at the front-end, nice imaging properties are provided by digital readout systems such as the one included in this MCM-based demonstrator.

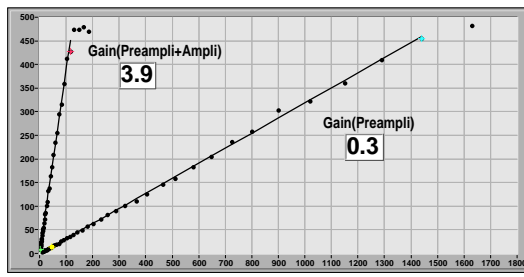


Fig. 16. Linearity in response of the overall readout chain without or with an additional amplification stage.

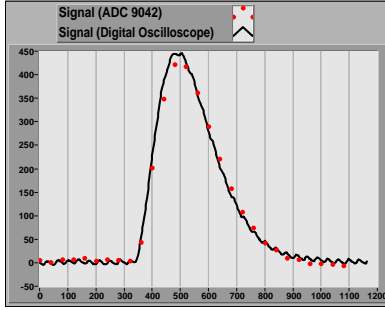


Fig. 17. Imaging properties of the MCM-based demonstrator as compared to a digital oscilloscope.

V. CONCLUSIONS

For the first time, a fast front-end digital readout including a performing low-noise and fast preamplifier, a fast and large dynamic range 12 bit-ADC, an integrated synchronization PLL and test cells, was designed and built using new I&P technologies, based here on an MCM-D packaging. The detailed tests achieved with this device, on various prototypes, show high performances in terms of noise, stability and reproducibility, signal processing and imaging properties.

Moreover, the high density and thus the reduction in space and connection length, the easy cooling, the integrated testability and therefore the reliability, the easy industrial production at large scale, and the relatively low cost, are among the appealing features of this new packaging technology as well as of the proposed readout system.

Various applications of the MCM-D packaging technology and of the proposed fast front-end digital readout scheme (or derivatives), are under study. The SUMMIT project studied a Global Positioning System (GPS) for industrial applications, and delivered a detailed GPS layout, with all the needed functions integrated in the active substrate [5]. The use of a fast front-end digital readout derived from the one presented here, is under evaluation for application to various medical imaging techniques. Finally,

this proposed system can serve as prototype for front-end readout systems for future HEP experiments and also for the next generation of astroparticle experiments, especially those embarked on satellites or spatial stations.

I&P technologies and early-stage digitization of the signal are certainly the way to go, to design highly performing front-end readout systems, in many industrial, biomedical as well as fundamental research applications, such as HEP and astroparticle physics.

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- [4] See data sheet of the AD9042 analog to digital converter by ANALOG Device.
- [5] The study and design of the layout of a GPS for industrial applications, was done by THOMSON-CSF DETEXIS, using the MCM-D technology and the appropriate cell libraries developed within the SUMMIT project.